REMARKS

Please note that the docket number for this case has been changed to 84,781. Please make the appropriate correction to the USPTO records.

Claims 1-41 are pending in the application. No claims are presently allowed.

The paragraph beginning at page 11, line 23 has been amended to include reference number 431 from amended Fig. 4.

Claims 1, 14, and 27 are amended to recite that the thread comprises instructions. Support for this amendment is found at page 8, lines 23-24.

Claims 1, 14, 27, 40, and 41 are amended to recite that the processing slice comprises a functional unit to perform a register operation specified in the instructions in each of the plurality of threads. Support for this amendment is found at page 12, lines 5-7.

Claims 1, 14, 27, 40, and 41 are amended to recite that the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle. Support for this amendment is found at page 8, lines 21-25.

Claims 12, 25, and 38 are amended to cancel the limitations regarding the functional unit. The limitations, in amended form, have been incorporated into the independent claims on which these claims depend.

Claims 12 and 38 are amended to change "the peripheral unit" to "a peripheral message unit" for consistency with Fig. 4. Support for this amendment is found in Fig. 4.

Claims 13, 26, and 39 are amended to cancel the limitation that the instructions are executed concurrently in a clock cycle. The limitation has been incorporated into the independent claims on which these claims depend.

Claim 26 has been amended to correct its claim dependency.

Claim 38 is amended to change the article "a" to "the" for elements having antecedent basis.

Claims 40 and 41 are amended to recite the limitation that a processor comprises a plurality of processor slices to execute a plurality of threads comprising instructions including the command message. The recitation "by a thread executing a message instruction" is cancelled as redundant. Support for this amendment is found at page 7 line 29 to page 8 line 1 and page 8 line 21-22.

Claims 4, 17, 24, 27, 30, and 41 are amended to correct spelling and grammar errors.

Drawings

The Examiner objected to the drawings for failing to show every feature of the invention specified in the claims. The drawings as filed did not show the register file's data registers from claims 12, 25, and 38. A replacement Fig. 4 is attached showing the data registers 431_0 to 431_3 as part of the register file 430.

The drawings do not show a coupling between the register file and the peripheral unit as had been recited in claims 12 and 38. These claims have been amended to recite that the register file is coupled to a peripheral message unit, as shown in Fig. 4.

Claim Objections

The Examiner objected to claims 4 and 17 as informal for reciting "the command messages includes." This has been corrected.

The Examiner objected to claim 24 as informal for reciting "thread b." This has been corrected.

The Examiner objected to claim 41 as informal for reciting "at least one peripheral units." This has been corrected.

Claim Rejections § 112

The Examiner rejected claims 12 (13 dependent thereon) and 25 under 35 U.S.C. § 112 second paragraph for reciting "an operation," when the element already had antecedent basis. The limitation containing this term has been cancelled.

The Examiner rejected claim 38 (39 dependent thereon) under 35 U.S.C. § 112 second paragraph for reciting "a plurality of data memories" and "a data memory switch," when these elements already had antecedent basis. The claim has been amended to change "the" to "a" in both cases.

The Examiner rejected claim 41 under 35 U.S.C. § 112 second paragraph for reciting "one of the multi-thread processors" and "one of the peripheral units," when these elements already had antecedent basis. The claim has been amended to cancel "one of" in both cases.

Claim Rejections § 102

The Examiner rejected claims 1-7, 9, 14-20, and 22 under 35 U.S.C. § 102 as anticipated by Bucher (US 5,421,014).

Claim 1 is to an apparatus comprising: a peripheral bus coupled to a peripheral unit and a processing slice coupled to the peripheral bus. The peripheral bus transfers peripheral information including a command message specifying a peripheral operation. The processing slice executes a plurality of threads comprising instructions. The threads include a first thread sending the command message to the peripheral unit. The processing slice comprises a functional unit to perform a register operation specified in the instructions in each thread. The processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

Bucher discloses a software architecture for implementing multi-thread control of a peripheral interface, especially a SCSI interface. The software operates at the driver level and manages multiple peripheral requests. A higher level program sends a peripheral request to the driver. When the operation is complete, the driver sends the result to the high level program. The high level program can continue its own execution without waiting for the result from the peripheral. (Col. 3, lines 22-35 and 52-63).

Bucher does not disclose the processing slice recited in claim 1. The processing slice is able to process several threads simultaneously, that is, instructions from two or more threads may be executing on the slice hardware at the same time. This is not the case with Bucher, which assumes a conventional processor in which instructions from just one thread are being executed at any time, and generally it takes several instruction executions to switch the processor from executing one thread to executing another thread. Claim 1 is not anticipated by Bucher. Claim 14 also recites the processing slice and is also not anticipated by Bucher.

Claims 2-7, 9, 15-20, and 22 depend from and contain all the limitations of claims 1 or 14 and are asserted to differ from the reference in the same way as claims 1 and 14.

Further, as to claims 9 and 22, the Examiner stated that Fig. 1 of Bucher shows loop backs that are equivalent to the non-wait instruction of the claims. Claims 9 and 22 recite that a thread continues to execute after sending a non-wait command message. However, Fig. 1 of Bucher does not show any activity of the threads. Threads are initiated in step 12 by issuing a command and terminated in step 16 by retrieving the results. The threads themselves are not

shown in this drawing. The looping is a higher level process that continuously polls to see if any commands/threads are either complete or pending, but is not a thread in itself. The threads are internal to the low level driver. Processes occurring outside the driver, as in Fig. 1 are not referred to as threads by Bucher.

Claim Rejections § 103

The Examiner rejected claims 8, 10-12, 21, 23-25, 27-38, 40, and 41 under 35 U.S.C. § 103 as unpatentable over the combination of Bucher and Motomura (US 5,815,727).

In order to make out a *prima facie* case of obviousness, each limitation of the claims must be disclosed in the references. Motomura discloses a parallel processor system for executing a plurality of threads. The system determines which thread is executed by each processor.

As in Bucher, Motomura does not disclose a processor slice as in claims 1 (8 and 10-12 dependent thereon), 14 (21 and 23-25 dependent thereon), 27, 40, and 41. The processor slice contains a functional unit to perform a register operation specified in the instructions in each of the plurality of threads. Thus, the functional unit is shared among multiple, simultaneously executing threads. Motomura does not disclose details of the processor, but it is known that a processor usually contains a unit for performing register operations. In Motomura, each executing thread has its own functional unit which does not perform operations from any other thread. Thus, each functional unit would have a significant amount of idle time. In the present invention, the functional unit is shared among the threads and is used more efficiently.

Further as to claim 40, the Examiner stated that Motomura discloses a plurality of multi-thread processors. However, Motomura discloses a plurality of single-thread processors.

Claims 8, 10-12, 21, 23-25, and 28-38 depend from and contain all the limitations of claims 1, 14, or 27 and are asserted to differ from the reference in the same way as claims 1, 14, and 27.

The Examiner rejected claims 13, 26, and 39 under 35 U.S.C. § 103 as unpatentable over the combination of Bucher, Motomura, and Hiraoka (US 5,418,917).

Hiraoka discloses a method and apparatus for controlling a conditional branch instruction in a pipeline type data processing apparatus. As in Bucher and Motomura, Hiraoka does not disclose a processor slice as recited in claims 1 (13 dependent thereon), 14 (26 dependent

thereon), and 27 (39 dependent thereon). Hiraoka discloses the execution of only one instruction at a time.

In view of the foregoing, it is submitted that the application is now in condition for allowance.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

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